Important notice

Dear Customer,

On 7 February 2017 the former NXP Standard Product business became a new company with the tradename **Nexperia**. Nexperia is an industry leading supplier of Discrete, Logic and PowerMOS semiconductors with its focus on the automotive, industrial, computing, consumer and wearable application markets

In data sheets and application notes which still contain NXP or Philips Semiconductors references, use the references to Nexperia, as shown below.

Instead of http://www.nxp.com, http://www.philips.com/ or http://www.semiconductors.philips.com/, use **http://www.nexperia.com**

Instead of sales.addresses@www.nxp.com or sales.addresses@www.semiconductors.philips.com, use **salesaddresses@nexperia.com** (email)

Replace the copyright notice at the bottom of each page or elsewhere in the document, depending on the version, as shown below:
- © NXP N.V. (year). All rights reserved or © Koninklijke Philips Electronics N.V. (year). All rights reserved
Should be replaced with:
- **© Nexperia B.V. (year). All rights reserved**.

If you have any questions related to the data sheet, please contact our nearest sales office via e-mail or telephone (details via **salesaddresses@nexperia.com**). Thank you for your cooperation and understanding,

Kind regards,

Team Nexperia

AN10343

MicroPak soldering information

Rev. 2 — 30 December 2010 Application note

Document information

Info	Content
Keywords	MicroPak, footprint, Ball Grid Array (BGA), Wafer-Level Chip Scale Package (WLCSP)
Abstract	This application note describes evaluation of recommended solder land patterns for mounting MicroPak packages

Revision history

Rev	Date	Description
v.2	20101230	text and graphics updated to latest standards

Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

1. Introduction

NXP Semiconductors' PicoGate and MicroPak packages are approximately ten to fifteen times smaller than conventional SO14 packages, providing significant miniaturization in space-constrained applications. They are available in a wide range of logic functions with a wide range of choices and deliver the right levels of performance.

PicoGate and MicroPak devices include single-, dual-, and triple-gate functions and are housed in 5-, 6-, 8- and 10-pin packages with selectable functions. To support the widest range of applications, every product in the portfolio is specified for high-temperature operation (−40 °C to +125 °C). Since they perform the most popular functions and either meet or exceed competitive specifications, they eliminate single-source problems.

Driven by applications with a very small circuit board mounting area, the PicoGate logic family offers the most popular logic functions for space-constrained systems such as cellular phones, pagers, and portable consumer products (CD players, VCRs, cameras, hard disks, notebook computers, PC cards, CD ROMs, and Personal Digital Assistants (PDAs)). They can also be used as simple glue/repair logic to implement last minute design changes or to eliminate dependence on intricate line layout patterns and to simplify routing.

This application note describes the following mounting methods for MicroPak packages:

- MicroPak footprint
- SOT886/833-1 MicroPak on WLCSP/BGA footprint and vice versa
- SOT996-2 MicroPak on VSSOP8 footprint and vice versa

2. MicroPak Overview

2.1 Package description

The MicroPak package is a near Chips Scale Package (CSP) Land Grid Array (LGA) type plastic encapsulated package with a copper lead frame base. The package has no leads or bumps with peripheral land terminals at the bottom of the package. The terminals are soldered to solder lands on the Printed-Circuit Board (PCB), after solder paste is deposited.

An overview of released MicroPak packages is given in Table 1.

Table 1. Overview MicroPak packages

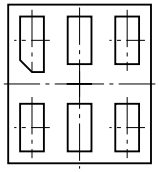
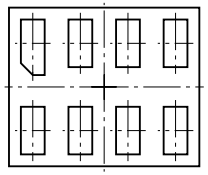
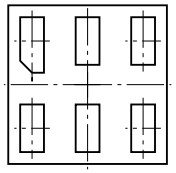
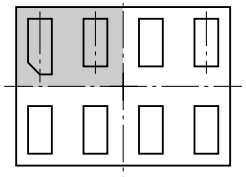
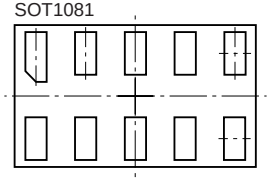
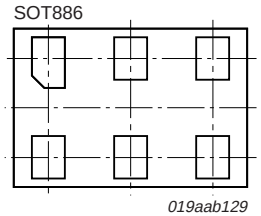
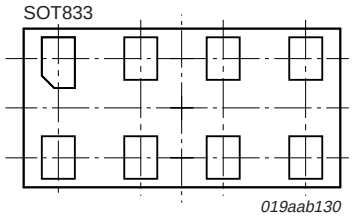
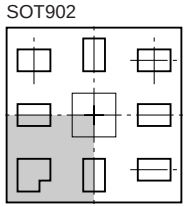
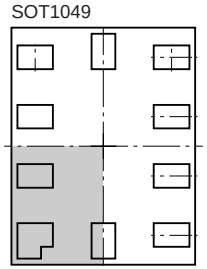
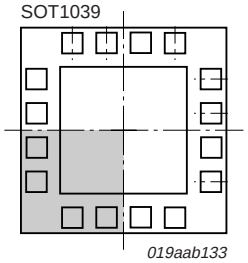
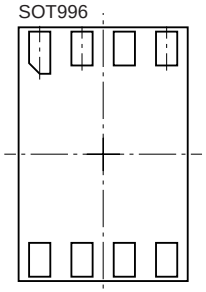
Properties		Number of pins			
Pitch [mm]	**Height [mm]**	**5 or 6**	**8**	**10**	**16**
0.3	0.35	SOT1115	SOT1116	-	-
		SOT1115  019aab124	SOT1116  019aab125		
0.35	0.5/0.35	SOT891/SOT1202	SOT1089/SOT1203	SOT1081-1	-
		SOT891/SOT1202  019aab126	SOT1089/SOT1203  019aab127	SOT1081  019aab128	

Table 1. Overview MicroPak packages *…continued*

Properties		Number of pins			
Pitch [mm]	**Height [mm]**	**5 or 6**	**8**	**10**	**16**
0.5 (Dual-in-Line)	0.5	SOT886  019aab129	SOT833-1  019aab130	-	-
0.5	0.5	-	SOT902-1  019aab131	SOT1049-1  019aab132	SOT1039-1  019aab133
0.5 (VSSOP8 replacement)	0.5	-	SOT996-2  019aab134	-	-

3. MicroPak soldering information

3.1 Solder paste

The following solder pastes were used in the evaluation and gave satisfactory results:

- PbSn paste: Alpha Metals Omnix 5002 (62 % Sn, 36 % Pb, 2 % Ag)
- SAC paste: Alpha Metals Omnix 310 (95.5 % Sn, 4 % Ag, 0.5 % Cu)

Both these solder pastes are 'no-clean'; due to the small stand-off height of the MicroPak, proper cleaning underneath the package is not possible.

Both Pb or Pb-free solder can be used, although it is advised to use Pb-free solder paste as this is required by European legislation from July 2006 onwards.

A wide variety of Pb-free solder pastes is available, containing combinations of tin, copper, antimony, silver, bismuth, indium, and other elements. The different types of Pb-free solder pastes have a wide range of melting temperatures. Solders with a high melting point may be more suitable for the automotive industry, whereas solders with a low melting point can be used for soldering consumer IC packages.

The most common substitute for SnPb solder, is Pb-free paste SAC, which is a combination of tin (Sn), silver (Ag), and copper (Cu). These three elements are usually in the range of 3 % to 4 % of Ag and 0 % to 1 % of Cu, which is near eutectic. SAC typically has a melting temperature of around 217 °C, and requires a reflow temperature of more than 235 °C.

Table 2. Typical solder paste characteristics

Solder (near eutectic alloys)	Melting temperature	Minimum peak reflow temperature
SnPb	183 °C	215 °C
SAC	217 °C	235 °C

A no-clean solder paste does not require cleaning after reflow soldering and is therefore preferred, provided that this is possible within the process window. If a no-clean paste is used, flux residues may be visible on the board after reflow.

For more information on the solder paste, please contact your solder paste supplier.

3.2 Moisture sensitivity level and storage

The MicroPak components have a very good package moisture resistance. The Moisture Sensitivity Level (MSL) according to JEDEC-STD-020D is MSL1.

Table 3. Pb-free process - Package classification reflow temperatures (from J-STD-020D)

Package thickness	Volume (<350 mm^3)	Volume (350 mm^3 to 2000 mm^3)	Volume (>2000 mm^3)
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm to 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

3.3 Stencil

Table 4 gives the recommended electroformed stencil thickness for MicroPak packages with a terminal pitch of greater than or equal to 0.5 mm, between 0.4 mm to 0.5 mm and less than or equal to 0.4 mm. Side wall roughness of the apertures should be smooth to improve the solder paste release.

Table 4. Typical stencil thicknesses

IC package pitch	Stencil thickness
≥0.5 mm	150 μm
0.4 mm to 0.5 mm	100 μm or 125 μm
≤0.4	100 μm

3.4 MicroPak placement

The required placement accuracy of a package depends on a variety of factors, such as package size and the terminal pitch, but also the package type itself. During reflow, when the solder is molten, a package that has not been placed perfectly may center itself on the pads: this is referred to as self-alignment. Therefore, the required placement accuracy of a package may be less tight if it is a trusted self-aligner. It is known, for example, that BGAs are good at self-alignment, as the package body essentially rests on a number of droplets of molten solder, resulting in minimal friction.

Table 5 gives typical placement tolerances as a function of the IC package terminal pitch.

Table 5. Typical placement accuracies

Package terminal pitch	Placement tolerance
≥0.65 mm	100 μm
<0.65 mm	50 μm

3.5 Reflow soldering

The most important step in reflow soldering is reflow itself, when the solder paste deposits melt and soldered joints are formed. This is achieved by passing the boards through an oven and exposing them to a temperature profile that varies in time. A temperature profile essentially consists of three phases:

1. Preheat: the board is warmed up to a temperature that is lower than the melting point of the solder alloy
2. Reflow: the board is heated to a peak temperature that is well above the melting point of the solder, but below the temperature at which the components and board's Organic Solderability Preservative (OSP) finish are damaged
3. Cooling down: the board is cooled down rapidly, so that soldered joints freeze before the board exits the oven

The peak temperature during reflow has an upper and a lower limit:

- Lower limit of peak temperature; the minimum peak temperature must be at least high enough for the solder to make reliable solder joints; this is determined by solder paste characteristics; contact your paste supplier for details
- The upper limit of the peak temperature must be lower than:

- the maximum temperature the component can withstand according to the specification
- the temperature at which the board or the components on the board are damaged (contact your board supplier for details)

Examples of a general purpose Pb-free reflow profile are shown is Figure 1 and Table 6.

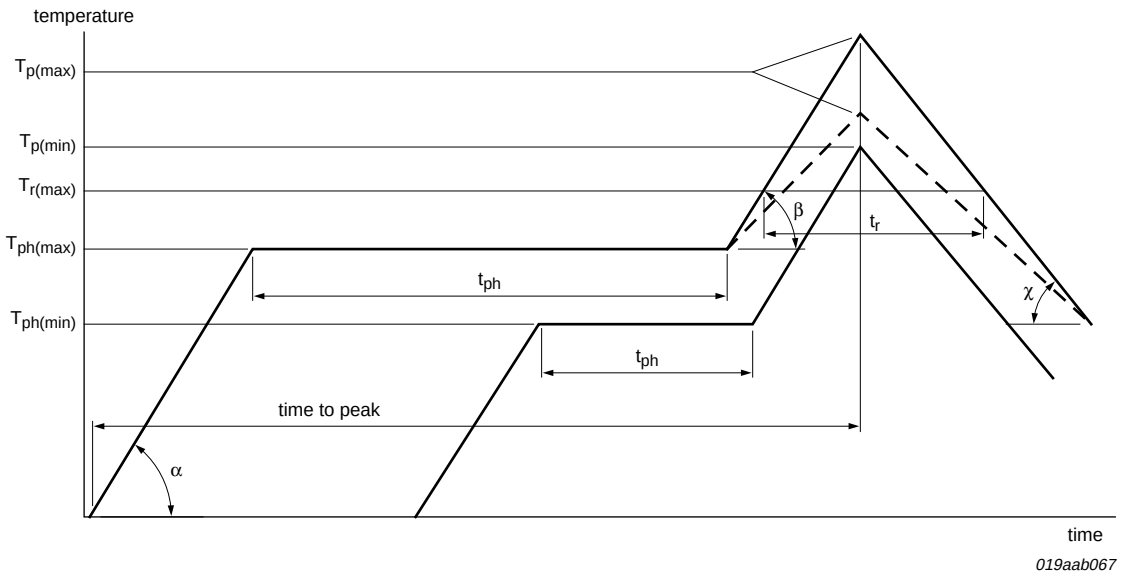


Fig 1. Example of a general purpose Pb-free reflow profile

Table 6. Explanation of the reflow temperature profile

Parameter	Value(s)	Typical value(s)	Remark
α	1 °C/s to 5 °C/s	2 °C/s	determined by component and board type and finish
ß	1°C/s to 5 °C/s	1.5 °C/s	determined by component and board type and finish
X	–2 °C/s to +6 °C	-	determined by component and board type and finish
$T_{ph(min)}$ to $T_{ph(max)}$	120 °C to 200 °C	160 °C	depends on the solder paste used - contact your solder paste supplier
t_{ph}	0 s to 180 s	100 s to 180 s	depends on the solder paste used - contact your solder paste supplier
t_r	30 s to 90 s	40 s to 70 s	depends on board finish and solder paste voiding behavior - contact your board and solder paste supplier
$T_{p(min)}$	235 °C	-	temperature measured in the solder at the coldest spot [1]
$T_{p(max)}$	260 °C	245 °C	depends on the board and the board finish in case of OSP and the most temperature-sensitive component used on the board [1]
reflow atmosphere	-	-	general purpose reflow is under air atmosphere, nitrogen reflow is allowed

[1] Delta between $T_{p(min)}$ and $T_{p(max)}$ preferably limited to 10 °C.

Additional soldering information and guidelines for board-mounting of surface-mount IC packages are described in *AN10365 'Surface mount reflow soldering description'*.

3.6 MicroPak soldering information for WLCSP/BGA footprint

Figure 2 shows the recommended solder land pattern for mounting the MicroPak XSON6 (SOT886) package. Using this pattern results in a very good electrical and mechanical connection which can also be inspected and tested for continuity. Using the land grid array package eliminates the co-planarity issues of leaded and WLCSP/BGA type devices.

The 6-pad MicroPak package available from NXP Semiconductors is alternately second-sourced by Fairchild Semiconductors. Although the footprint for the Texas Instruments WLCSP/BGA package is physically smaller, the MicroPak very easily fits the same footprint. Figure 3 shows the recommended solder land pattern for the WLCSP/BGA package and the footprint of the MicroPak SOT886.

Placing the WLCSP/BGA package on the MicroPak footprint is not recommended. As can be seen in Figure 4, the larger land pattern for the MicroPak may cause solder starvation due to the limited amount of solder in the package solder ball. Solder paste would help, although there will be limited mechanical contact. This is true for the larger Pb-free WLCSP/BGA balls. Even less mechanical contact is achieved with the smaller PbSn WLCSP/BGA balls. Figure 5 shows the recommended solder land pattern for the WLCSP/BGA package and the footprint of the MicroPak SOT833-1.

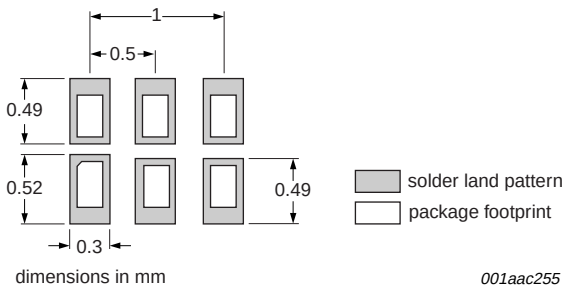


Fig 2. MicroPack footprint

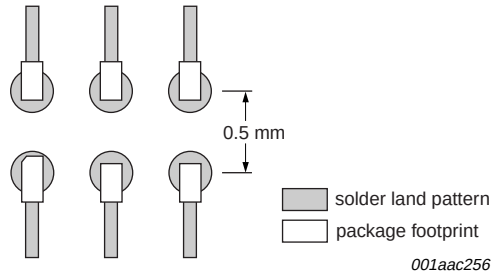


Fig 3. MicroPack SOT886 on BGA footprint

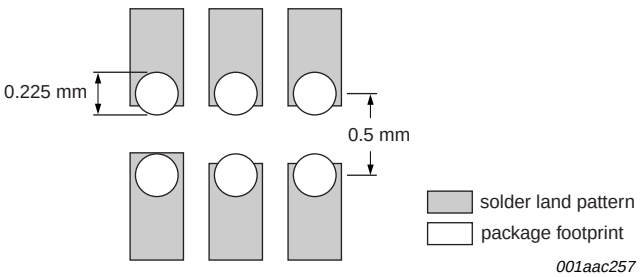


Fig 4. BGA on MicroPack footprint

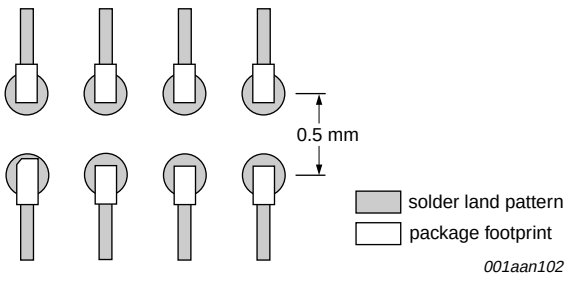
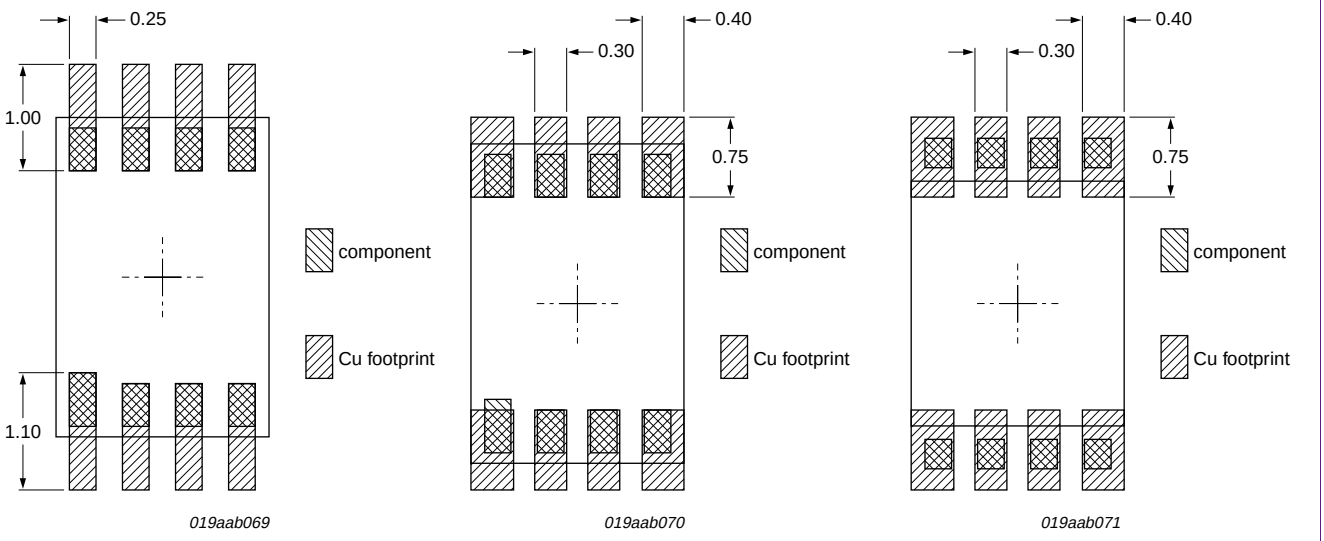


Fig 5. MicroPack SOT833-1 on BGA footprint

3.7 SOT996-2 MicroPak soldering information for VSSOP8 footprint

Figure 6a shows the recommended solder land pattern footprint for mounting the MicroPak XSON8 (SOT996-2) package. Using this pattern results in a very good electrical and mechanical connection which can also be inspected and tested for continuity. Figure 6b shows how the MicroPak XSON8 (SOT996-2) package fits the VSSOP8 (SOT765-1) solder land pattern footprint. Figure 6c shows the VSSOP8 (SOT765-1) package on its VSSOP8 solder land pattern footprint.



a. XSON8/SOT996-2 package superimposed on its recommended solder land pattern footprint

b. XSON8/SOT996-2 package superimposed on solder land pattern footprint for VSSOP8/SOT765-1

c. VSSOP8/SOT765-1 package superimposed on its solder land pattern footprint

Fig 6. Solder land pattern footprints for mounting package MicroPak XSON8U (SOT996-2)

4. Manual repair of leadless MicroPak

In general, replacing a defective component on a soldered board, during repair or rework, can be carried out either manually or with a dedicated repair station.

The rework process should consist of the following steps:

1. Dry bake the board and the new component, if necessary
2. Mark the position of the old component
3. Remove the old component
4. Prepare the site
5. Print solder paste on the new component
6. Reflow the solder paste on the new component
7. Place the new component on the board
8. Solder the new component
9. Visual inspection, electrical measurement, and X-ray inspection

The above steps are summarized in Figure 7.

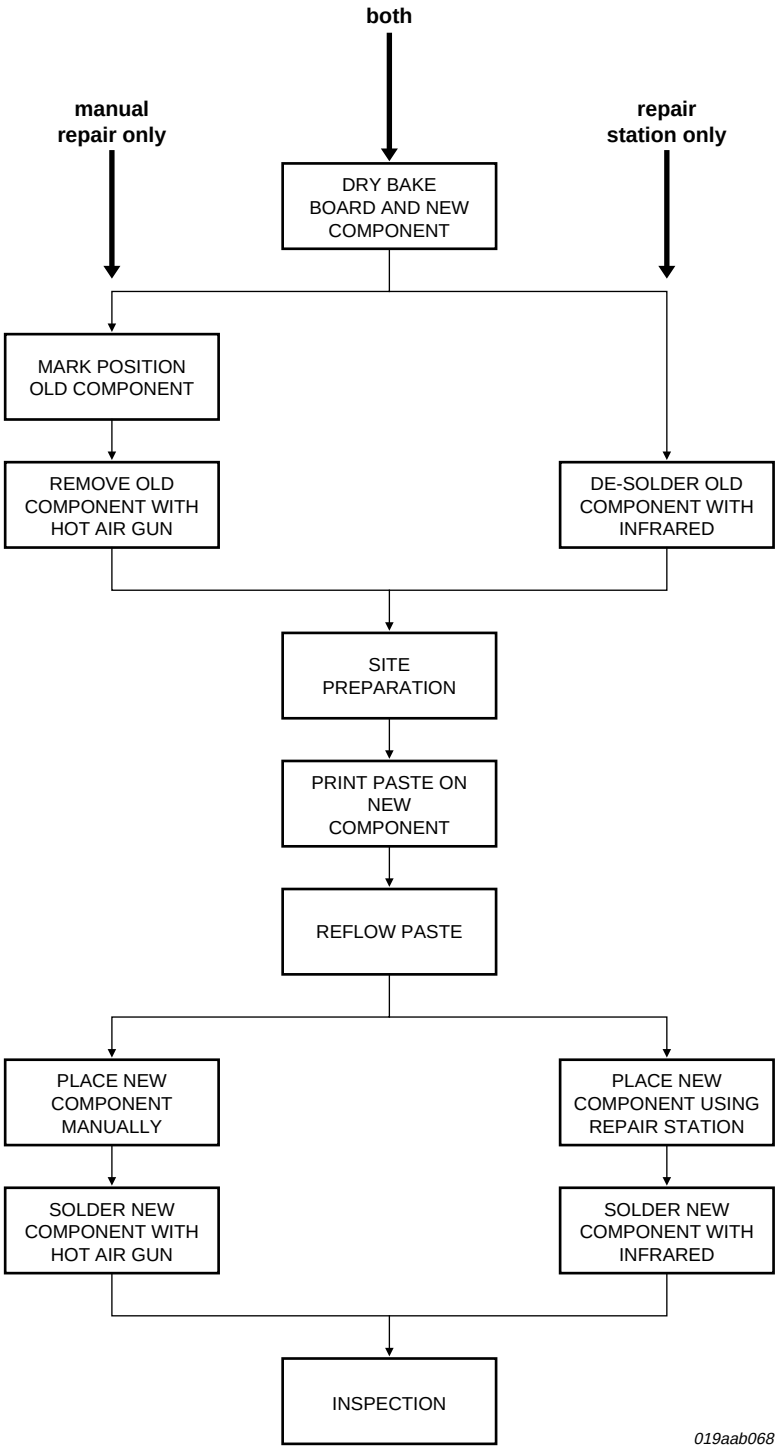
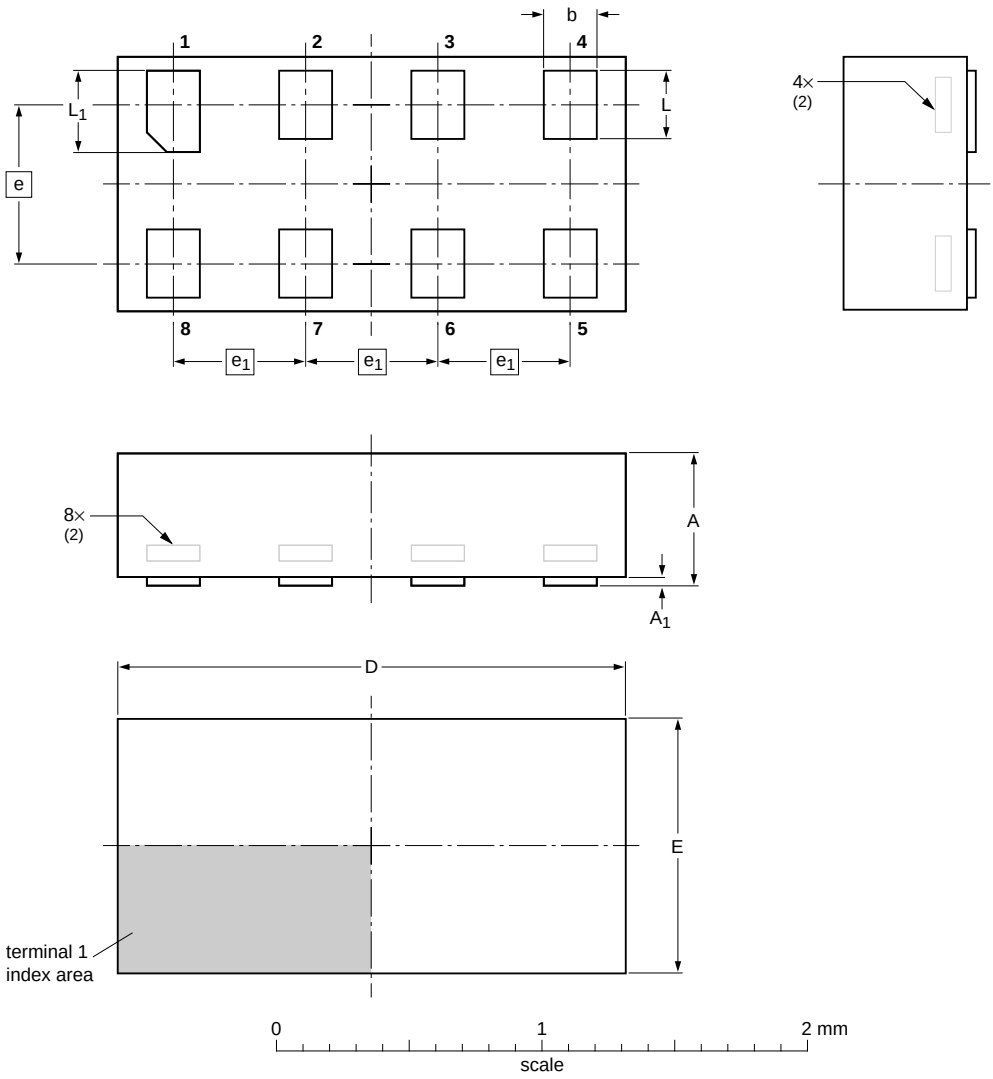


Fig 7. Rework process steps

5. Package outline and PCB footprint

The package outline drawing and recommended soldering footprint of the released packages are shown in Figure 10 to Figure 19. The soldering footprints are only recommended and may be different for specific application requirements.

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 8. SOT833-1 (XSON8) package outline

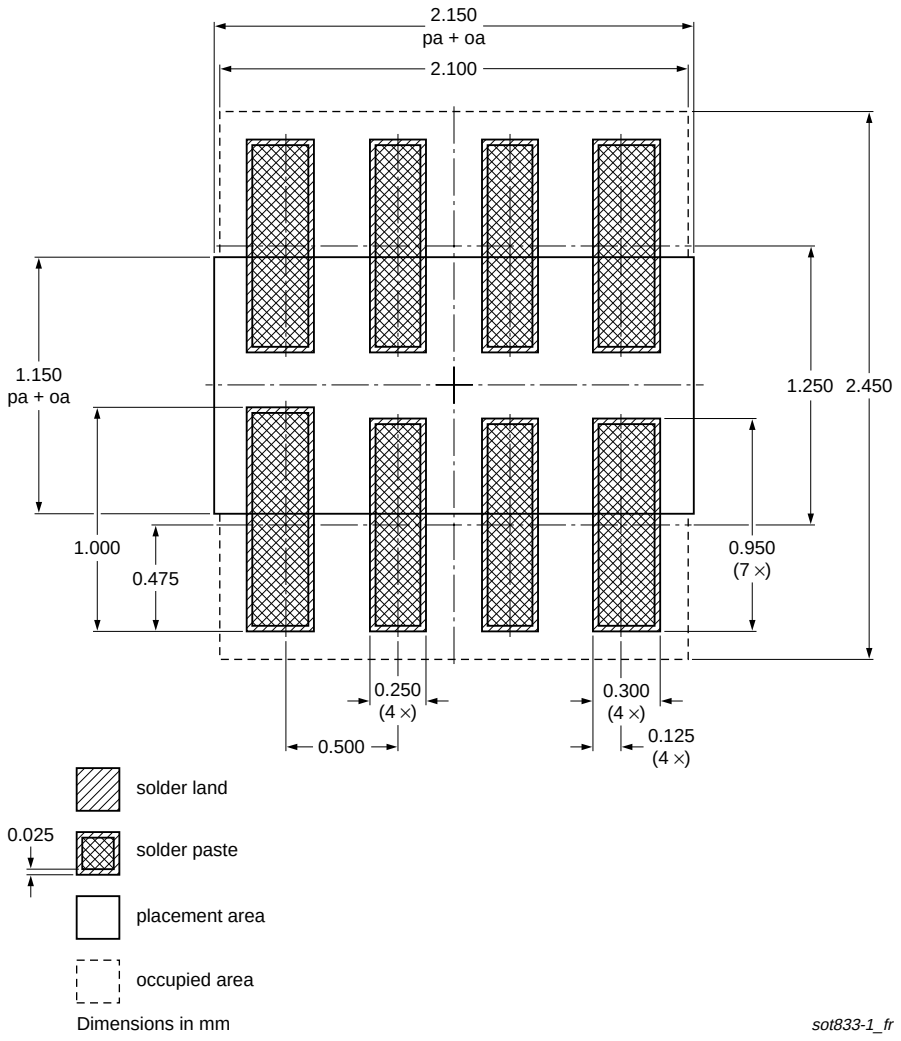
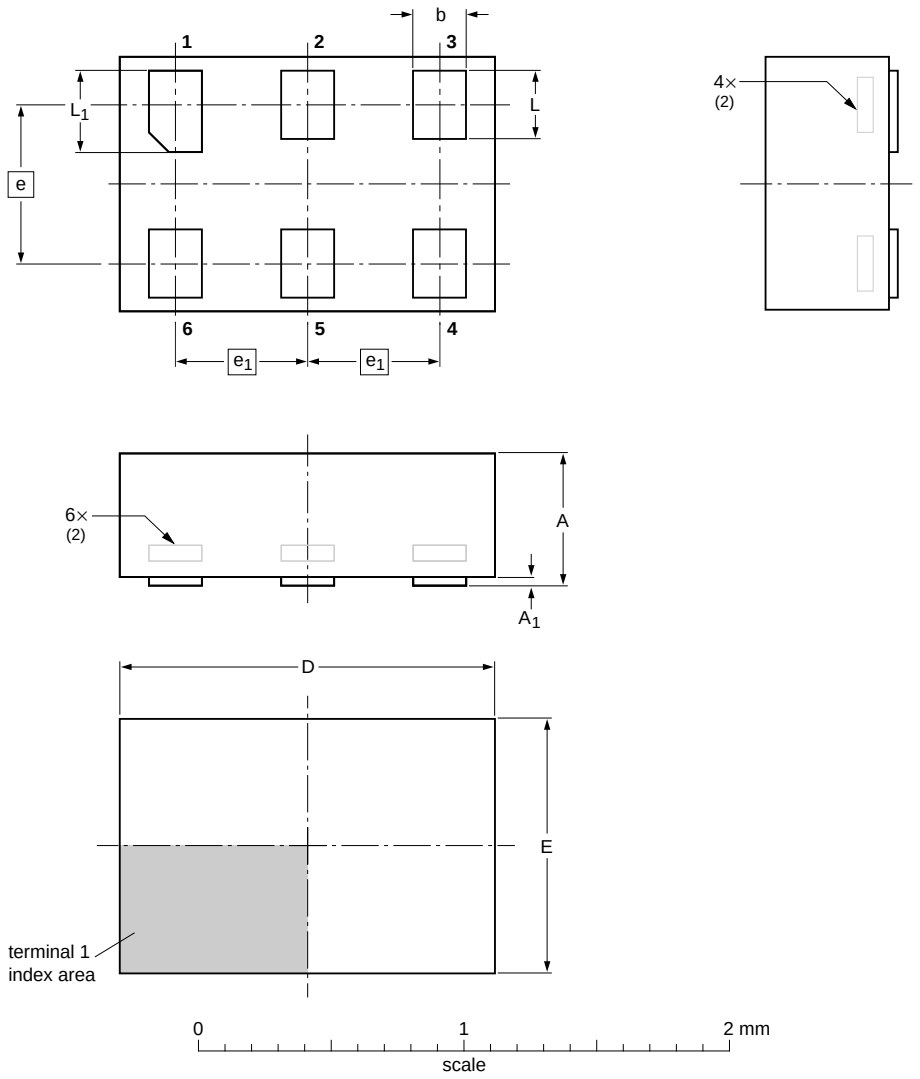


Fig 9. SOT833-1 (XSON8) solder footprint

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A1 max	b	D	E	e	e1	L	L1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

Fig 10. SOT886 (XSON6) package outline

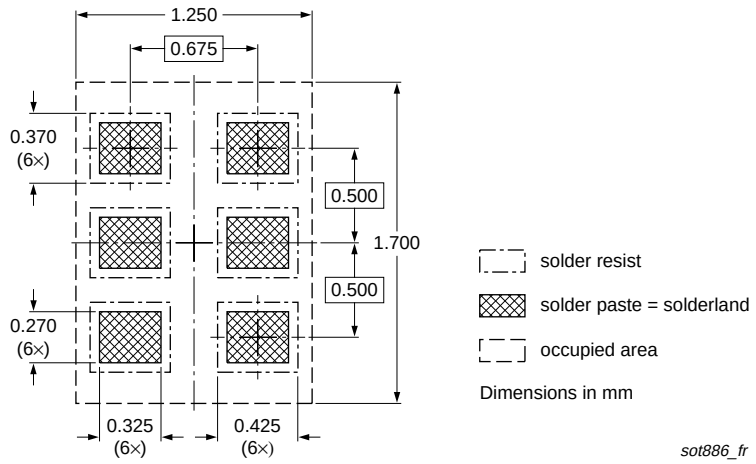
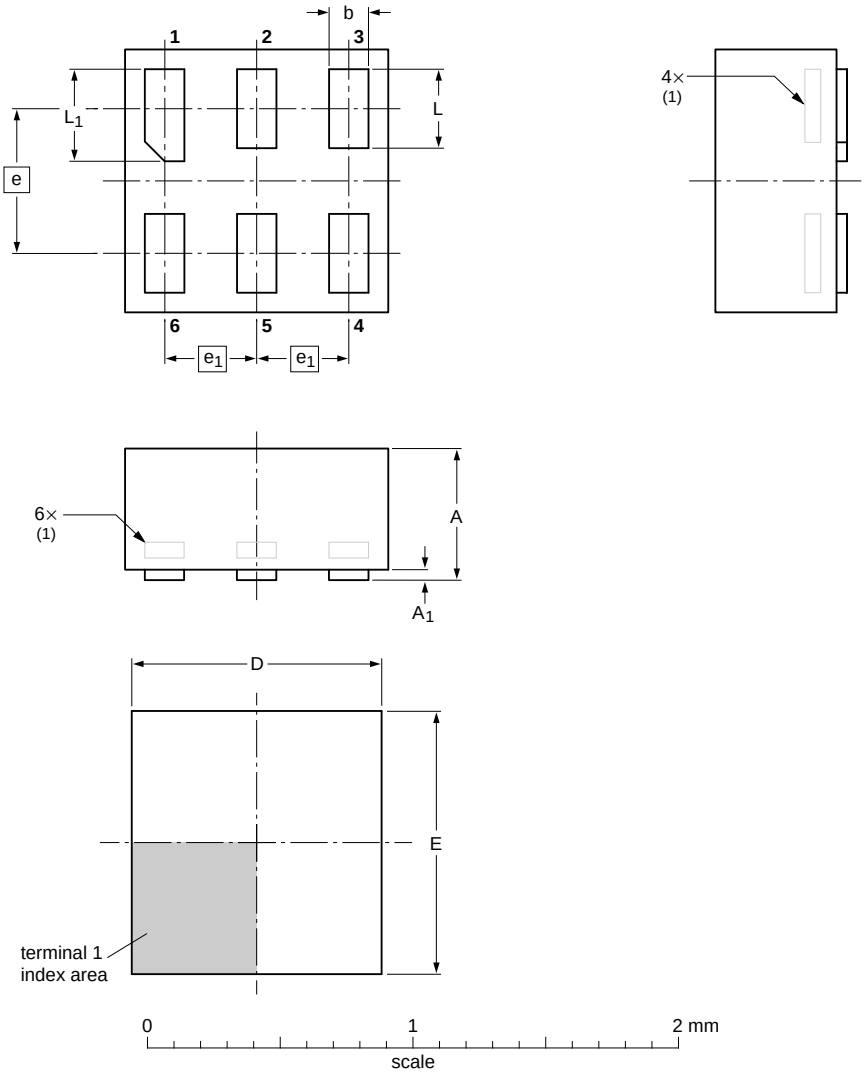


Fig 11. SOT886 (XSON6) solder footprint

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm **SOT891**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.20 0.12	1.05 0.95	1.05 0.95	0.55	0.35	0.35 0.27	0.40 0.32

Note

1. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT891						~~05-04-06~~ 07-05-15

Fig 12. SOT891 (XSON6) package outline

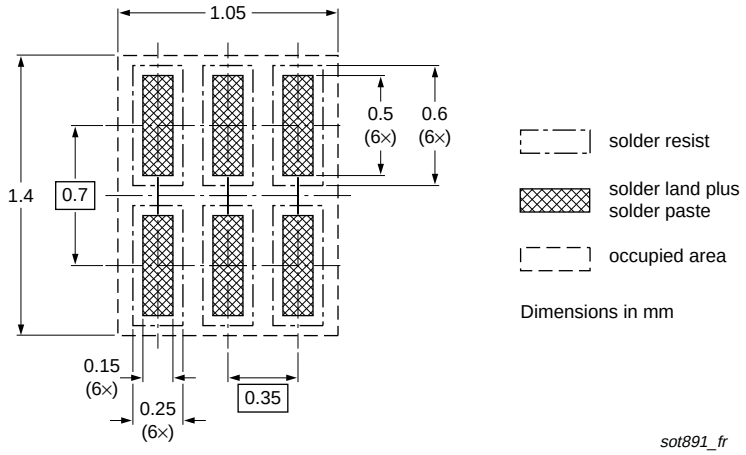
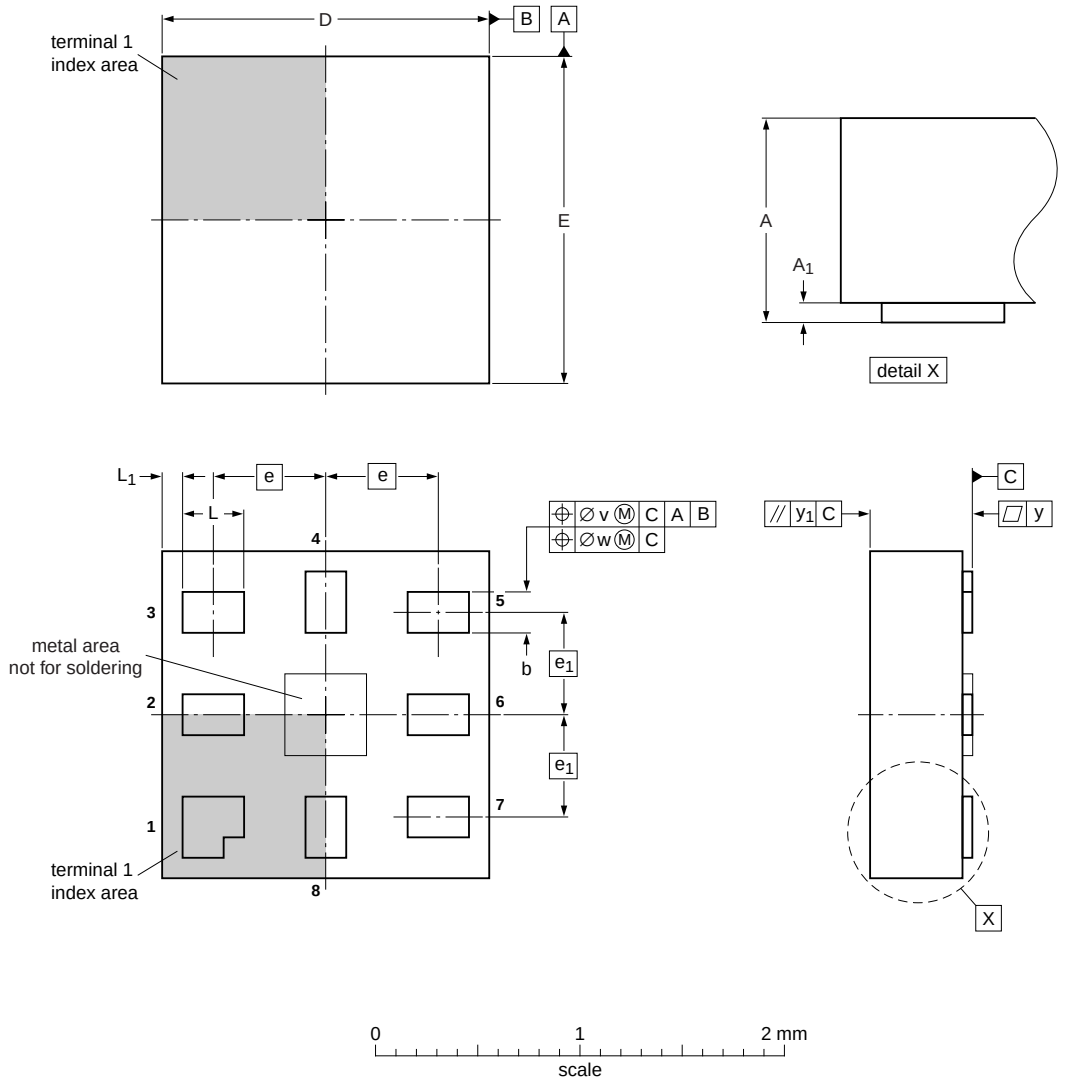


Fig 13. SOT891 (XSON6) solder footprint

XQFN8U: plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm **SOT902-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT902-1	- - -	MO-255	- - -			~~05-11-25~~ 07-11-14

Fig 14. SOT902-1 (XQFN8U) package outline

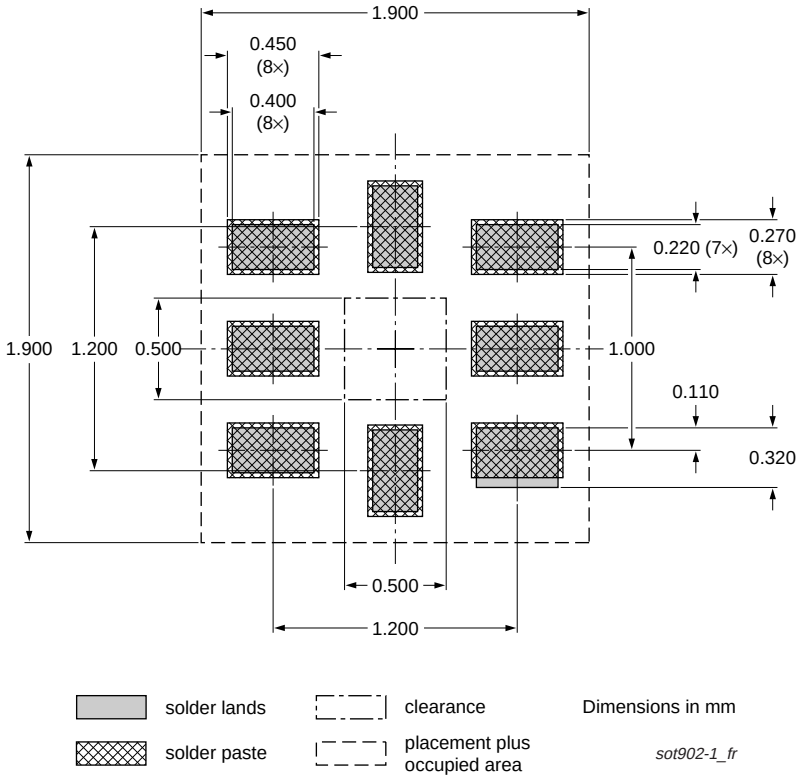
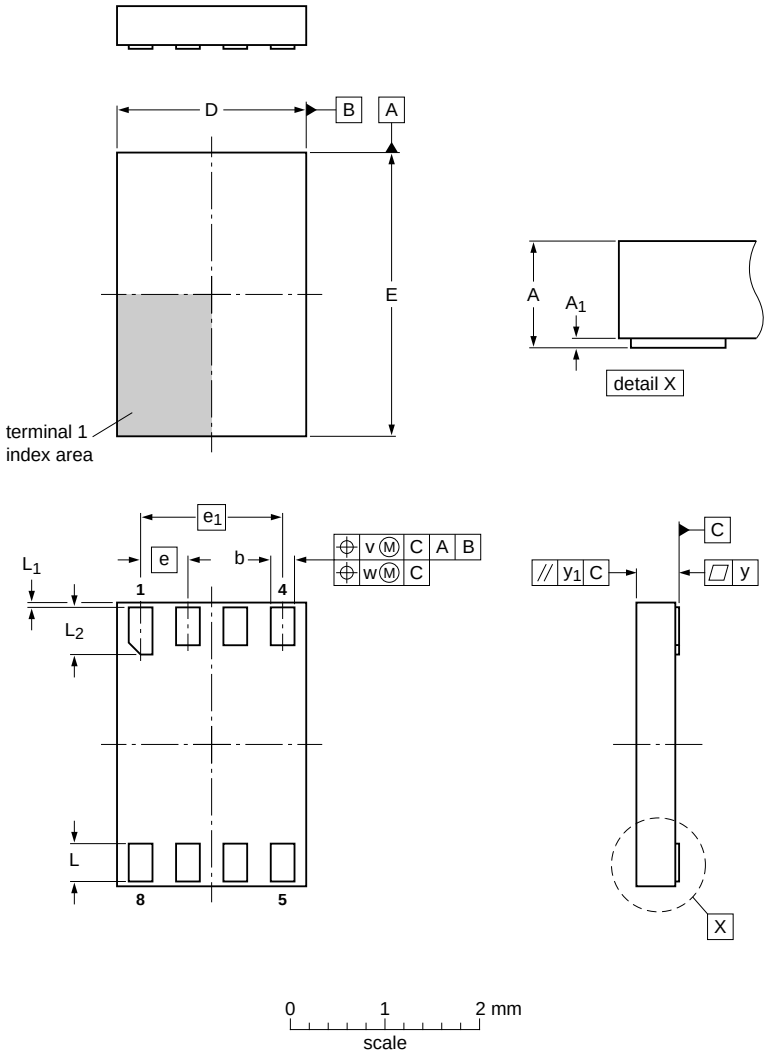


Fig 15. SOT902-1 (XQFN8U) solder footprint

XSON8U: plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 x 2 x 0.5 mm **SOT996-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	L_2	v	w	y	y_1
mm	0.5	0.05 0.00	0.35 0.15	2.1 1.9	3.1 2.9	0.5	1.5	0.5 0.3	0.15 0.05	0.6 0.4	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT996-2	- - -		- - -			~~07-12-18~~ 07-12-21

Fig 16. SOT996-2 (XSON8U) package outline

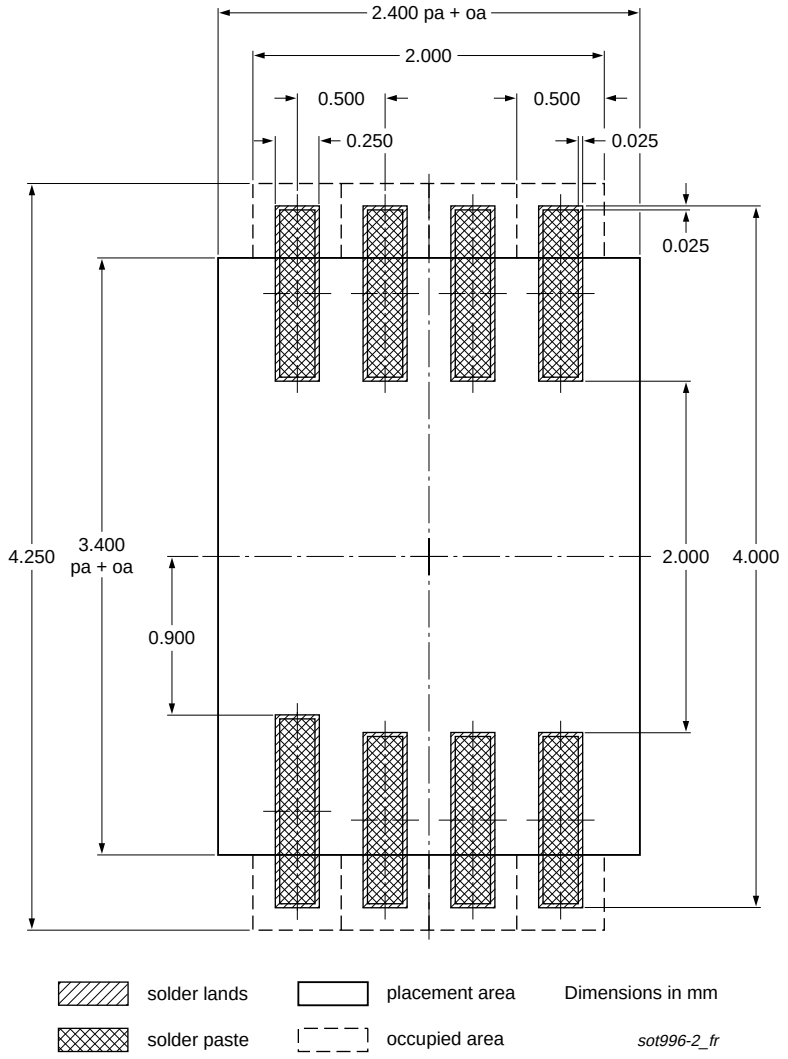
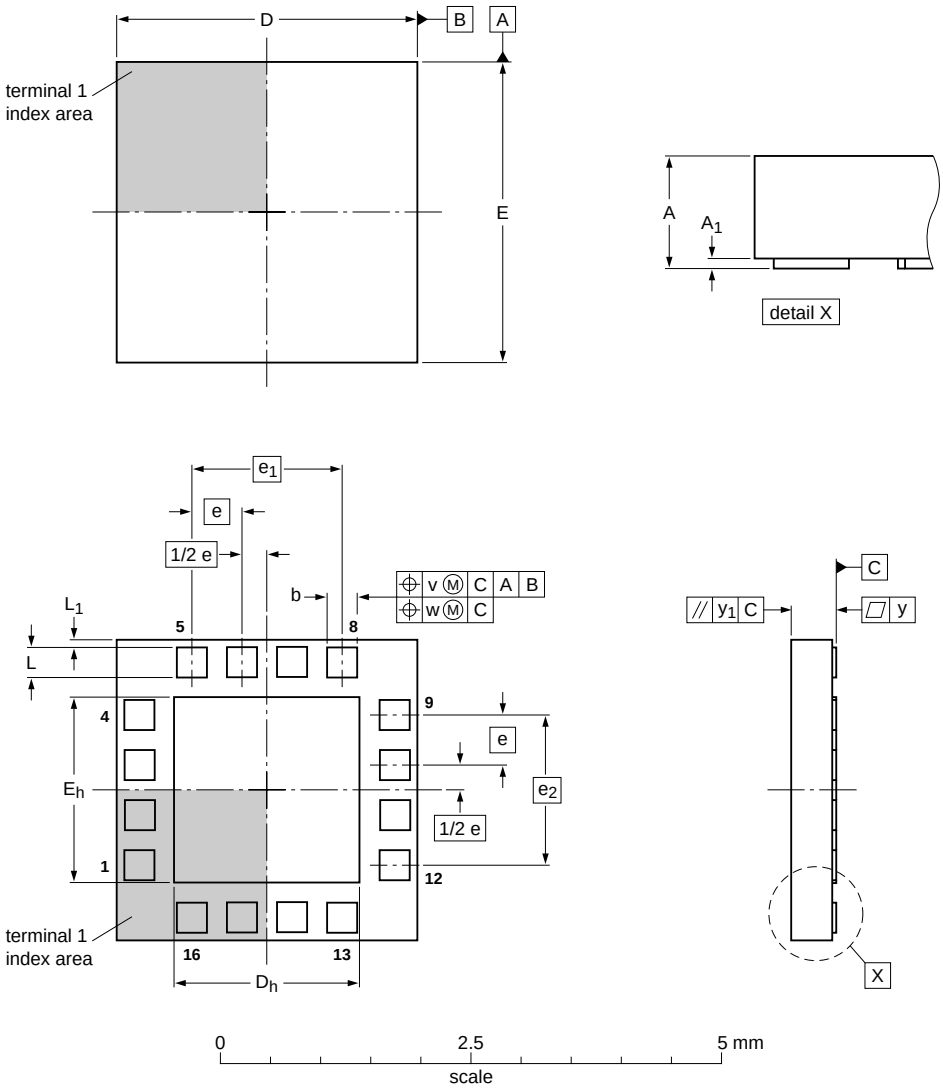


Fig 17. SOT996-2 (XSON8U) solder footprint

HXQFN16U: plastic thermal enhanced extremely thin quad flat package; no leads; 16 terminals; UTLP based; body 3 x 3 x 0.5 mm **SOT1039-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	D_h	E	E_h	e	e_1	e_2	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.35 0.25	3.1 2.9	1.95 1.75	3.1 2.9	1.95 1.75	0.5	1.5	1.5	0.35 0.25	0.1 0.0	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1039-1	- - -		- - -			~~07-11-14~~ 07-12-01

Fig 18. SOT1039-1 (HXQFN16U) package outline

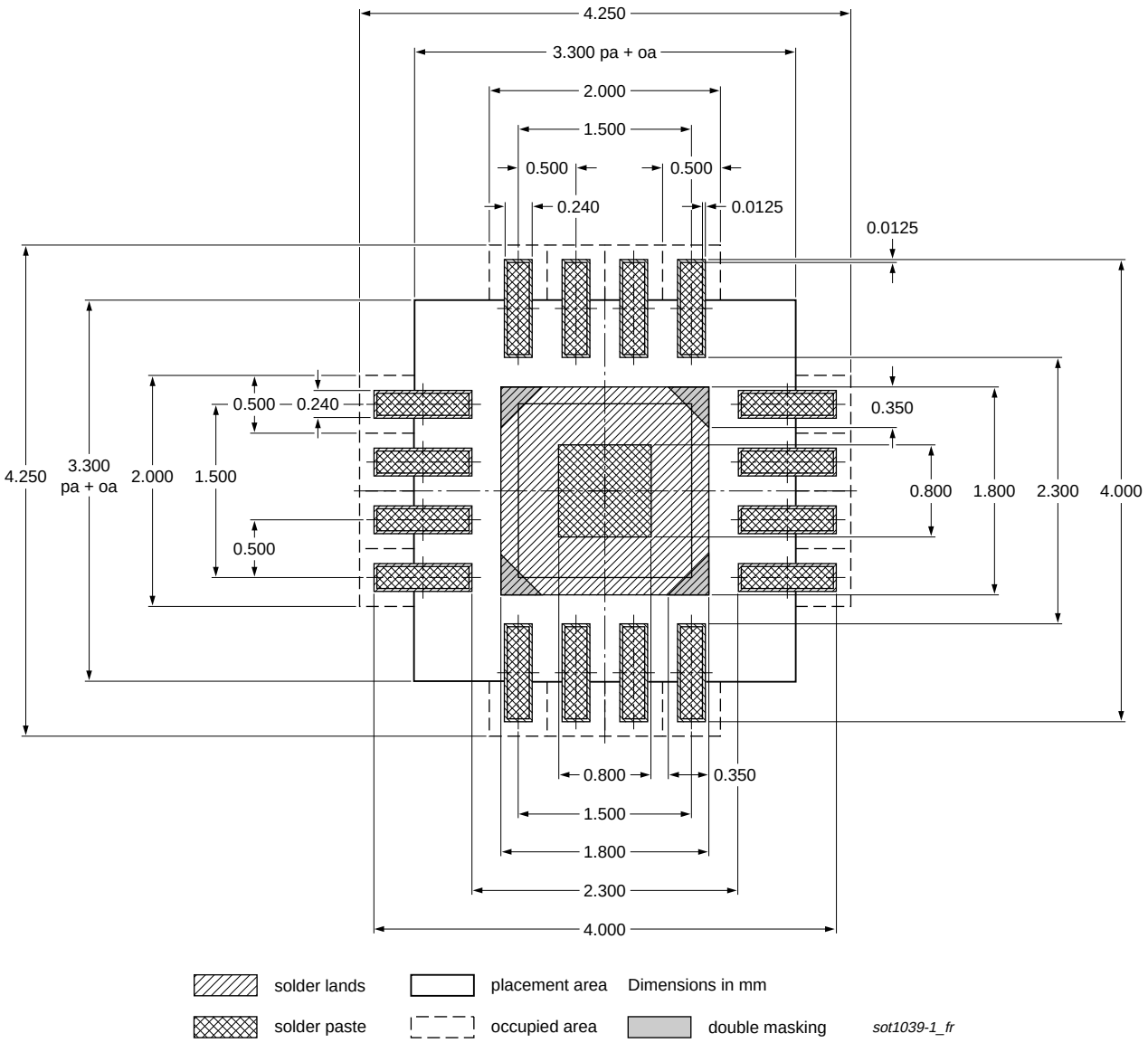
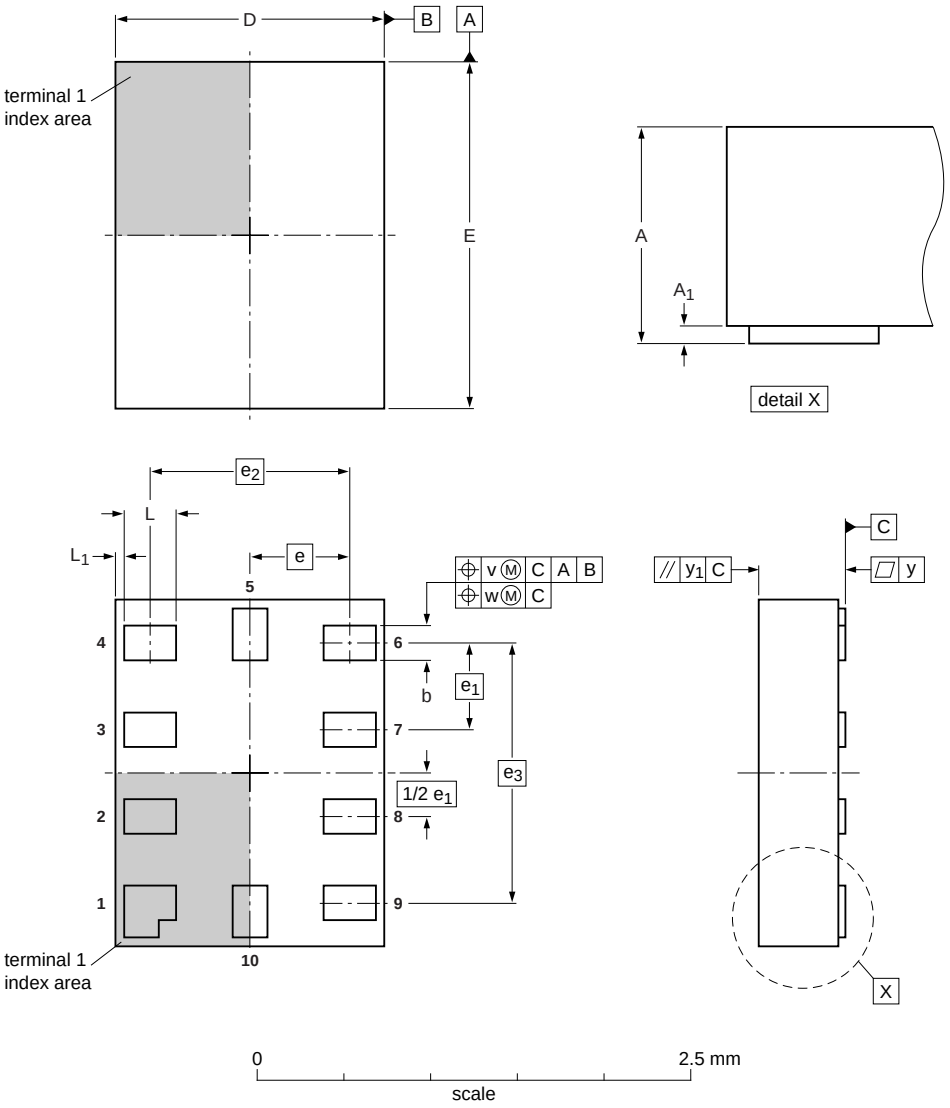


Fig 19. SOT1039-1 (HXQFN16U) solder footprint

XQFN10U: plastic extremely thin quad flat package; no leads; 10 terminals; UTLP based; body 2 x 1.55 x 0.5 mm **SOT1049-1**



DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	b	D	E	e	e_1	e_2	e_3	L	L_1	v	w	y	y_1
mm	max	0.50	0.05	0.30	1.65	2.1	0.58	0.5	1.16	1.5	0.4	0.15	0.1	0.05	0.1	0.05
	nom		0.03	0.23	1.55	2.0					0.3	0.08				
	min		0.00	0.15	1.45	1.9					0.2	0.00				

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1049-1	- - -	MO-255	- - -			~~08-02-28~~ 10-02-05

Fig 20. SOT1049-1 (XQFN10U) package outline

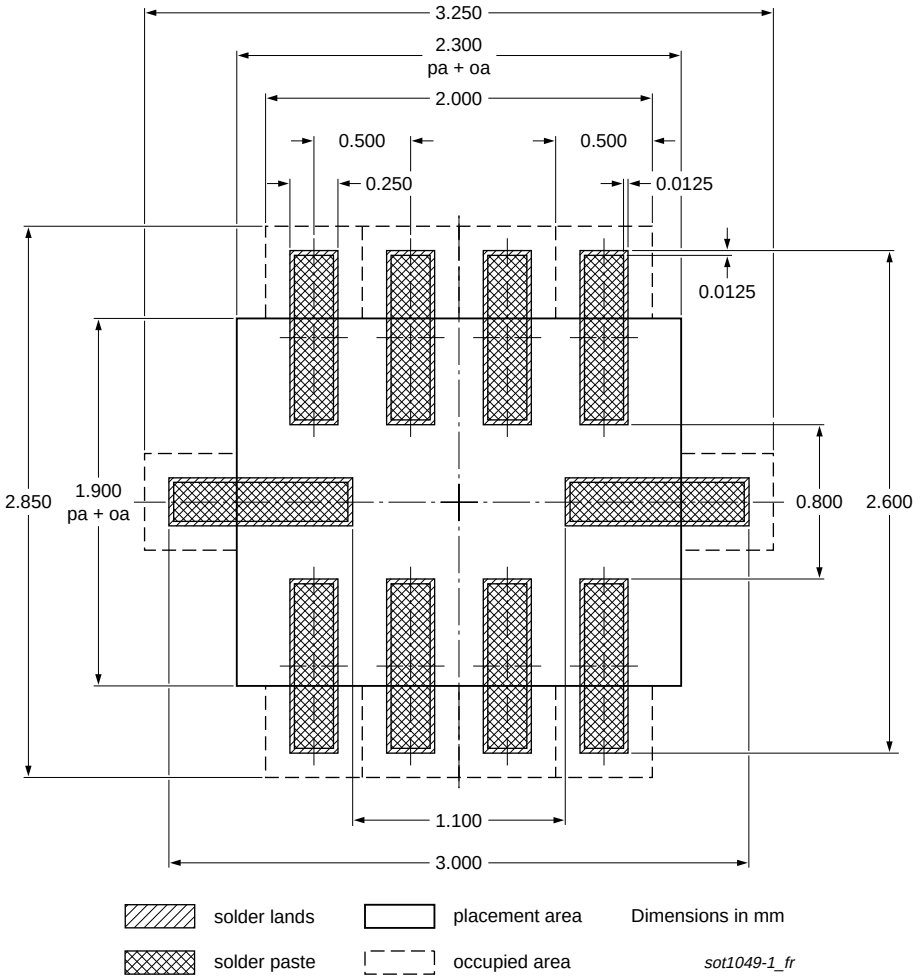
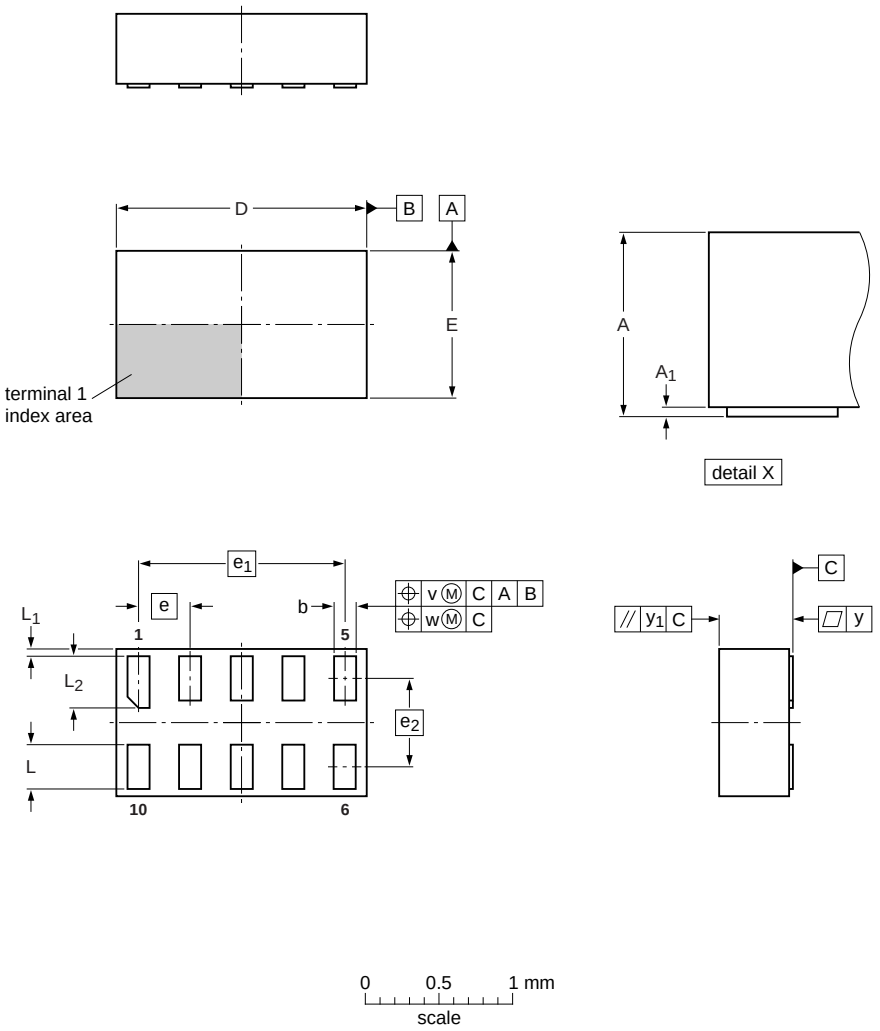


Fig 21. SOT1049-1 (XQFN10U) solder footprint

XSON10U: plastic extremely thin small outline package; no leads; 10 terminals; UTLP based; body 1 x 1.7 x 0.5 mm **SOT1081-1**



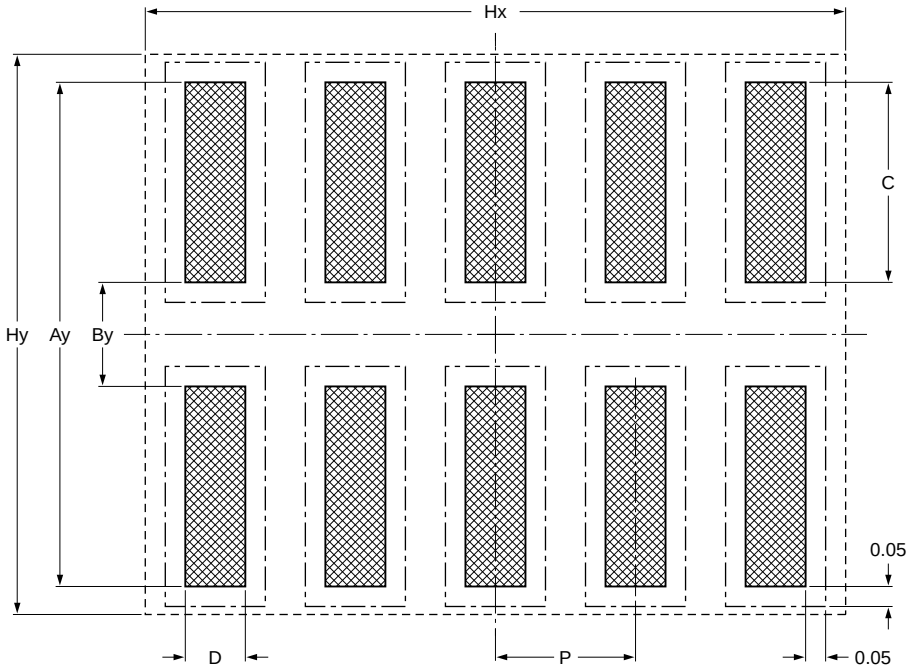
DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	b	D	E	e	e_1	e_2	L	L_1	L_2	v	w	y	y_1
mm	max	0.50	0.05	0.20	1.8	1.1				0.4	0.10	0.45				
	nom	0.48	0.03	0.15	1.7	1.0	0.35	1.4	0.6	0.3	0.05	0.35	0.1	0.05	0.05	0.1
	min	0.46	0.00	0.10	1.6	0.9				0.2	0.00	0.25				

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1081-1	- - -		- - -			~~08-03-28~~ 08-04-18

Fig 22. SOT1081-1 (XSON10U) package outline

Footprint information for reflow soldering of XSON10U package **SOT1081-1**



Generic footprint pattern

Refer to the package outline drawing for actual layout

solder land

solder paste deposit

solder land plus solder paste

occupied area

solder resist

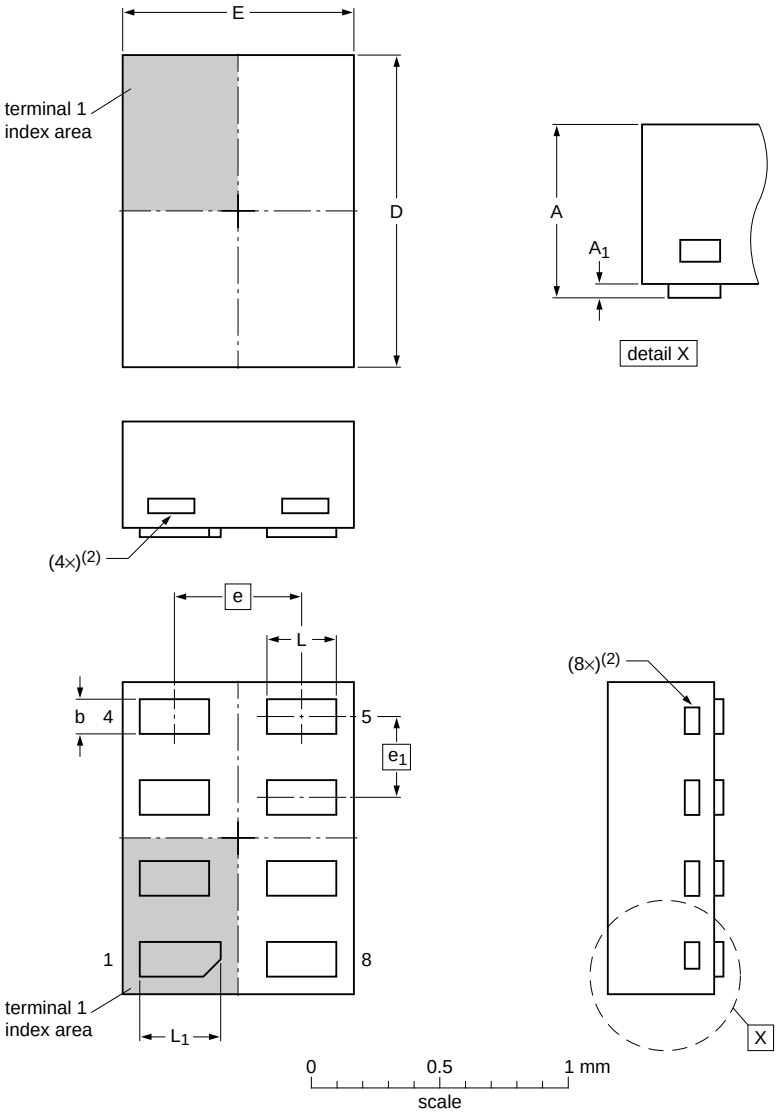
Dimensions in mm

P	Ay	By	C	D	Hx	Hy
0.35	1.26	0.26	0.5	0.15	1.75	1.4

Remark:
Stencil of 75 µm is recommended.
A stencil of 75 µm gives an aspect ratio of 0.77
With a stencil of 100 µm one will obtain an aspect ratio of 0.58

Fig 23. SOT1081-1 (XSON10U) solder footprint

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1 x 0.5 mm **SOT1089**



Dimensions

Unit		A(1)	A1	b	D	E	e	e1	L	L1
	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
mm	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				~~10-04-09~~ 10-04-12

Fig 24. SOT1089 (XSON8) package outline

Footprint information for reflow soldering of XSON8 package **SOT1089**

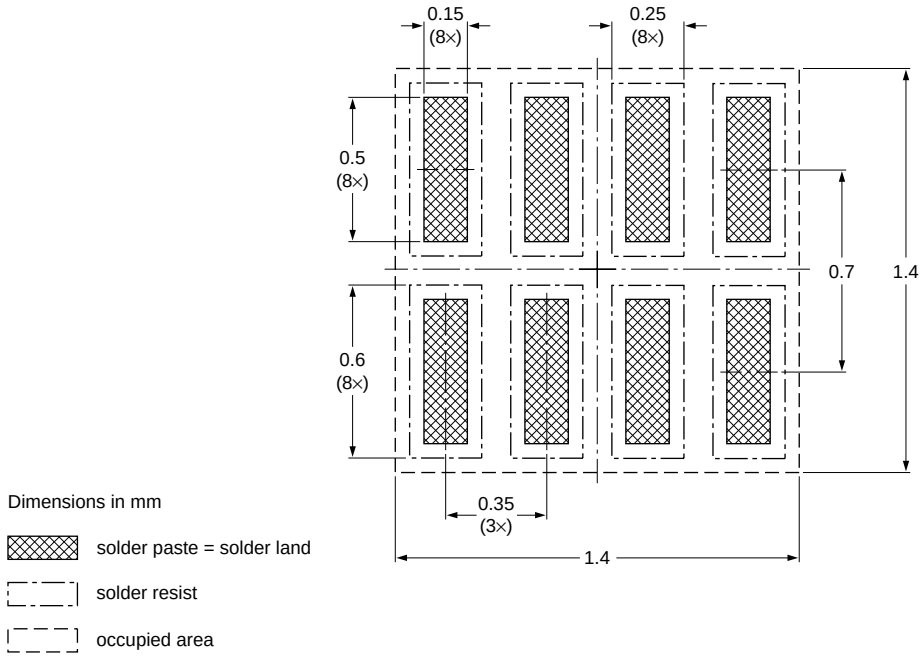


Fig 25. SOT1089 (XSON8) solder footprint

6. Legal information

6.1 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

6.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

6.3 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

7. Contents

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 30 December 2010
Document identifier: AN10343